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10/813,834	03/31/2004	Keiichiro Tounai	NEC A433	6044

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HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE, SUITE 140
TUCSON, AZ 85718

EXAMINER	
PARK, EDWARD	

ART UNIT	PAPER NUMBER
2624	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,834	TOUNAI, KEIICHIRO	
	Examiner	Art Unit	
	EDWARD PARK	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This action is responsive to applicant's amendment and remarks received on 4/7/08. Claims 1-26 are currently pending.

Claim Rejections - 35 USC § 101

2. In response to applicant's amendment of claims 8-14, the previous claim rejection is withdrawn.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1, 2, 3, 8, 9, 10, 15, 16, 17, 21-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Garza et al (US 5,705,301) in view of Kamon (US 6,453,274 B2).

Regarding **claims 1, 2, 3**, Garza discloses a method of testing a mask pattern, comprising the steps of:

applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer (see figure 5c; col. 11, lines 40-46; col. 1, lines 63-67; col. 2, lines 1-7 corrected IC layout design through optical proximity correction);

dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer (see figure 5b; col. 8, lines 41-62 divided into grid regions where OPC sequentially operates on each grid region);

determining sampling points on an edge of said first pattern (figure 5c, col. 11, lines 40-46);

simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern (see col. 13, lines 11-21). Garza does not disclose determining a test standard for each of said areas; checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs, wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other; sampling points, is determined in accordance with a N-the process in said step (c) wherein N indicates an integer equal to or greater than one (N = 1,2,3,4, ---), and first to N-th processes are different from one another; and dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

Kamon, in the same field of endeavor, teaches determining a test standard for each of said areas (see figure 5, numeral S3; col. 5, lines 14-31 pattern prediction unit 4 predicts the size of a pattern which will be finally obtained after a pattern transfer process); checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs, wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other (see figure 5, numeral s6; col. 5, lines 14-47 determination unit 7 determines whether correction amount is within the predefined allowable range); sampling points, is determined in accordance with a N-th process in said step (c) wherein N indicates an integer equal to or greater than one (N = 1,2,3,4, ---), and first to N-th processes are different from one another (see figures 8b, 9b; col. 8, lines 45-67; col. 9, lines 1-7); and dividing an edge of said first pattern into a plurality of portions (see figure 8b), wherein said test standard is determined for each of said portions (see figure 5, numeral S3).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Garza reference to utilize a test standard and different processes as taught by Kamon, to allow the "final pattern size [to have] a required accuracy" (col. 5, lines 48-55) and "great reduction in correction time" (col. 8, lines 50-55) which is essential in mask/reticle fabrication.

Regarding **claims 8, 9, 10**, Garza discloses a computer-readable medium storing a program for causing a computer to carry out a method of testing a mask pattern (figure 3, numerals 252, 271, 268, 269, 271, 256, 258 general purpose computer system representing one of many suitable computer platforms for implementing the inventive optical proximity correction

methods), wherein said method is executed by said computer in accordance with said program including the steps of:

applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer (see figure 5c; col. 11, lines 40-46; col. 1, lines 63-67; col. 2, lines 1-7 corrected IC layout design through optical proximity correction);

dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer (see figure 5b; col. 8, lines 41-62 divided into grid regions where OPC sequentially operates on each grid region);

determining sampling points on an edge of said first pattern (figure 5c, col. 11, lines 40-46);

simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern (see col. 13, lines 11-21). Garza does not disclose determining a test standard for each of said areas; checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs, wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other; sampling points, is determined in accordance with a N-th process in said step (c) wherein N indicates an integer equal to or greater than one (N = 1,2,3,4, ---), and first to N-th processes are different from one another; and dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

Kamon, in the same field of endeavor, teaches determining a test standard for each of said areas (see figure 5, numeral S3; col. 5, lines 14-31 pattern prediction unit 4 predicts the size of a pattern which will be finally obtained after a pattern transfer process); checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs, wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other (see figure 5, numeral s6; col. 5, lines 32-47 determination unit 7 determines whether correction amount is within the predefined allowable range); sampling points, is determined in accordance with a N-th process in said step (c) wherein N indicates an integer equal to or greater than one (N = 1,2,3,4, ---), and first to N-th processes are different from one another (see figures 8b, 9b; col. 8, lines 45-67; col. 9, lines 1-7); and dividing an edge of said first pattern into a plurality of portions (see figure 8b), wherein said test standard is determined for each of said portions (see figure 5, numeral S3).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Garza reference to utilize a test standard and different processes as taught by Kamon, to allow the "final pattern size [to have] a required accuracy" (col. 5, lines 48-55) and "great reduction in correction time" (col. 8, lines 50-55) which is essential in mask/reticle fabrication.

Regarding **claim 15, 16, 17**, Garza discloses a method of forming a mask having a desired mask pattern including the steps of:

applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer (see figure

5c; col. 11, lines 40-46; col. 1, lines 63-67; col. 2, lines 1-7 corrected IC layout design through optical proximity correction);

dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer (see figure 5b; col. 8, lines 41-62 divided into grid regions where OPC sequentially operates on each grid region);

determining sampling points on an edge of said first pattern (figure 5c, col. 11, lines 40-46);

simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern (see col. 13, lines 11-21); and transferring said mask pattern onto a mask (see col. 11, lines 60-67 IC layout design 600 may be transferred onto an actual glass and chromium (or other material) reticle). Garza does not disclose determining a test standard for each of said areas; checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs, wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other; sampling points, is determined in accordance with a N-th process in said step (c) wherein N indicates an integer equal to or greater than one (N = 1,2,3,4, ---), and first to N-th processes are different from one another; and dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

Kamon, in the same field of endeavor, teaches determining a test standard for each of said areas (see figure 5, numeral S3; col. 5, lines 14-31 pattern prediction unit 4 predicts the size of a pattern which will be finally obtained after a pattern transfer process); checking whether a

dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs, wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other (see figure 5, numeral s6; col. 5, lines 32-47 determination unit 7 determines whether correction amount is within the predefined allowable range); sampling points, is determined in accordance with a N-th process in said step (c) wherein N indicates an integer equal to or greater than one (N = 1,2,3,4, ---), and first to N-th processes are different from one another (see figures 8b, 9b; col. 8, lines 45-67; col. 9, lines 1-7); and dividing an edge of said first pattern into a plurality of portions (see figure 8b), wherein said test standard is determined for each of said portions (see figure 5, numeral S3).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Garza reference to utilize a test standard and different processes as taught by Kamon, to allow the "final pattern size [to have] a required accuracy" (col. 5, lines 48-55) and "great reduction in correction time" (col. 8, lines 50-55) which is essential in mask/reticle fabrication.

Regarding **claim 21**, Garza further discloses a gate layer, and a number of sampling points in an area acting as a gate of a transistor is higher than the same in other areas (see col. 4, lines 65-67; col. 5, lines 1-10; locations on the integrated circuit pattern chosen for correction correspond to locations where field oxide feature edges on a field oxide integrated circuit pattern intersect gate electron feature edges on a layout design undergoing correction for reflective notching).

Regarding **claim 22**, Garza further discloses a gate layer, and a number of sampling points in a contact area is higher than the same in other areas (see col. 4, lines 65-67; col. 5, lines 1-10; locations on the integrated circuit pattern chosen for correction correspond to locations where field oxide feature edges on a field oxide integrated circuit pattern intersect gate electron feature edges on a layout design undergoing correction for reflective notching).

Regarding **claim 23**, Garza further discloses a gate layer, and a number of sampling points in an area acting as a gate of a transistor is higher than the same in other areas (see col. 4, lines 65-67; col. 5, lines 1-10; locations on the integrated circuit pattern chosen for correction correspond to locations where field oxide feature edges on a field oxide integrated circuit pattern intersect gate electron feature edges on a layout design undergoing correction for reflective notching).

Regarding **claim 24**, Garza further discloses a gate layer, and a number of sampling points in a contact area is higher than the same in other areas (see col. 4, lines 65-67; col. 5, lines 1-10; locations on the integrated circuit pattern chosen for correction correspond to locations where field oxide feature edges on a field oxide integrated circuit pattern intersect gate electron feature edges on a layout design undergoing correction for reflective notching).

Regarding **claim 25**, Garza further discloses a gate layer, and a number of sampling points in an area acting as a gate of a transistor is higher than the same in other areas (see col. 4, lines 65-67; col. 5, lines 1-10; locations on the integrated circuit pattern chosen for correction correspond to locations where field oxide feature edges on a field oxide integrated circuit pattern intersect gate electron feature edges on a layout design undergoing correction for reflective notching).

Regarding **claim 26**, Garza further discloses a gate layer, and a number of sampling points in a contact area is higher than the same in other areas (see col. 4, lines 65-67; col. 5, lines 1-10; locations on the integrated circuit pattern chosen for correction correspond to locations where field oxide feature edges on a field oxide integrated circuit pattern intersect gate electron feature edges on a layout design undergoing correction for reflective notching).

5. **Claims 4, 5, 11, 12, 18, 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Garza et al (US 5,705,301) with Kamon (US 6,453,274 B2), and further in view of Tounai et al (US 2002/0043615 A1).

Regarding **claims 4 and 5**, Garza with Kamon combination discloses all elements as mentioned above in claim 1. Garza with Kamon combination does not teach a first pattern that is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer; and third area is comprised of said contact area and an ambient area surrounding said contact area.

Tounai teaches a first pattern that is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer (figure 13; paragraphs [0093]-[0096]); and third area is comprised of said contact area and an ambient area surrounding said contact area (figure 13; paragraphs [0093]-[0096]).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Garza with Kamon combination to utilize a first pattern, second pattern, and

a third area as suggested by Tounai, to fabricate/simulate a mask pattern and to increase reliability of correcting an optical proximity effect of the section around the contact area.

Regarding **claims 11 and 12**, Garza with Kamon combination discloses all elements as mentioned above in claim 8. Garza with Kamon combination does not teach a first pattern that is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer; and third area is comprised of said contact area and an ambient area surrounding said contact area.

Tounai teaches a first pattern that is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer (figure 13; paragraphs [0093]-[0096]); and third area is comprised of said contact area and an ambient area surrounding said contact area (figure 13; paragraphs [0093]-[0096]).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Garza with Kamon combination to utilize a first pattern, second pattern, and a third area as suggested by Tounai, to fabricate/simulate a mask pattern and to increase reliability of correcting an optical proximity effect of the section around the contact area.

Regarding **claims 18 and 19**, Garza with Kamon combination discloses all elements as mentioned above in claim 15. Garza with Kamon combination does not teach a first pattern that is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in

which said contact makes contact with said wiring layer; and third area is comprised of said contact area and an ambient area surrounding said contact area.

Tounai teaches a first pattern that is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer (figure 13; paragraphs [0093]-[0096]); and third area is comprised of said contact area and an ambient area surrounding said contact area (figure 13; paragraphs [0093]-[0096]).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Garza with Kamon combination to utilize a first pattern, second pattern, and a third area as suggested by Tounai, to fabricate/simulate a mask pattern and to increase reliability of correcting an optical proximity effect of the section around the contact area.

6. **Claims 6, 7, 13, 14, 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Garza et al (US 5,705,301) with Kamon (US 6,453,274 B2), and further in view of Magoshi et al (US 6,316,163 B1).

Regarding **claims 6 and 7**, Garza with Kamon combination discloses all elements as mentioned above in claim 1. Garza with Kamon combination does not teach a first pattern that is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern, and a fourth area that is comprised of said fifth area and an ambient area surrounding said fifth area.

Magoshi teaches a first pattern that is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS

transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern, and a fourth area that is comprised of said fifth area and an ambient area surrounding said fifth area (figure 2; Magoshi: col. 5, lines 58-67; col. 6, lines 1-13).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Garza with Kamon combination to utilize a first pattern for forming a wiring layer, second pattern for forming an active area, and a fourth area comprised of a fifth area and an ambient area as suggested by Magoshi, to perform the steps of "forming patterns involving pattern transfer to the same photosensitive material" (Magoshi: col. 8, lines 32-45).

Regarding **claims 13 and 14**, Garza with Kamon combination discloses all elements as mentioned above in claim 8. Garza with Kamon combination does not teach a first pattern that is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern, and a fourth area that is comprised of said fifth area and an ambient area surrounding said fifth area.

Magoshi teaches a first pattern that is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern, and a fourth area that is comprised of said fifth area and an ambient area surrounding said fifth area (figure 2; Magoshi: col. 5, lines 58-67; col. 6, lines 1-13).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Garza with Kamon combination to utilize a first pattern for forming a wiring layer, second pattern for forming an active area, and a fourth area comprised of a fifth area and an ambient area as suggested by Magoshi, to perform the steps of "forming patterns involving pattern transfer to the same photosensitive material" (Magoshi: col. 8, lines 32-45).

Regarding **claim 20**, Garza with Kamon combination discloses all elements as mentioned above in claim 15. Garza with Kamon combination does not teach a first pattern that is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern.

Magoshi teaches a first pattern that is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern (figure 2; Magoshi: col. 5, lines 58-67; col. 6, lines 1-13).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Garza with Kamon combination to utilize a first pattern for forming a wiring layer, and second pattern for forming an active area as suggested by Magoshi, to perform the steps of "forming patterns involving pattern transfer to the same photosensitive material" (Magoshi: col. 8, lines 32-45).

Response to Arguments

7. Applicant's arguments filed 4/7/08, in regards to **claims 1, 8, and 15**, have been fully considered but they are not persuasive. Applicant argues that neither the Kamon or Garza disclose a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other (see pg. 8, second paragraph). This argument is not considered persuasive since it can be seen in Kamon (col. 5, lines 14-47), that the pattern prediction unit 4 predicts the size of a pattern which will be finally obtained after a pattern transfer process; the comparison unit 5 compares the predicted pattern size with the size of the design pattern which was input via the design comparison unit 1 and outputs a correction amount which is a difference between the predicted pattern size and the design value. It can be seen in figure 5, numeral s6 that if a correction amount is not within an allowable range then the steps are repeated (S3-S5), which would create another different test standard for a second area at figure 5, numeral S3 to be compared to the design data.

Regarding **claims 2-7, 9-14, and 16-20**, applicant argues that these claims are allowable due to the dependency on claims 1, 8 and 15 respectively. (see pg. 8, third paragraph). This argument is not considered persuasive since claims 1, 8, and 15 still stand rejected and the argument and rejection can be seen above.

Regarding **claims 4, 5, 11, 12, 18, 19**, applicant argues that these claims are allowable due to the dependency on claims 1 , 8, or 15 respectively. (see pg. 9, first paragraph). This

argument is not considered persuasive since claims 1, 8, and 15 still stand rejected and the argument and rejection can be seen above.

Regarding **claims 6, 7, 13, 14, 20**, applicant argues that these claims are allowable due to the dependency on claims 1 , 8, or 15 respectively. (see pg. 9, second paragraph). This argument is not considered persuasive since claims 1, 8, and 15 still stand rejected and the argument and rejection can be seen above.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWARD PARK whose telephone number is (571)270-1576. The examiner can normally be reached on M-F 10:30 - 20:00, (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vikkram Bali can be reached on (571) 272-7415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Edward Park
Examiner
Art Unit 2624

/Edward Park/
Examiner, Art Unit 2624

/Vikkram Bali/
Supervisory Patent Examiner, Art Unit 2624